



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/287,776	04/07/1999	LILI KANG	0100.9900270	6690

7590 11/06/2003

CHRISTOPHER J. RECKAMP
MARKISON & RECKAMP, P.C.
P. O. BOX 06229
WACKER DRIVE
CHICAGO, IL 606060229

EXAMINER

PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
2673	23

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No.

09/287,776

Applicant(s)

KANG ET AL.

Examiner

Jeff Piziali

Art Unit

2673

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 06 October 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
(a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
(b) ☐ they raise the issue of new matter (see Note below);
(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☐ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

Claim(s) objected to: _____

Claim(s) rejected: _____

Claim(s) withdrawn from consideration: _____

8. ☐ The proposed drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.
10. ☐ Other: _____


J.P.

4 November 2003

Continuation of 5. does NOT place the application in condition for allowance because: Applicants' arguments filed 6 October 2003 have been fully considered but they are not persuasive.

Firstly, the applicants contend the cited prior art of Ranganathan (US 5,764,201) neglects to disclose a switching mechanism that functions to switch video data into one of two display devices. However, the examiner respectfully disagrees. Ranganathan explicitly discloses a programmable switching mechanism [Fig. 8A; 68 working in conjunction with 67] to switch video data [Fig. 8A; output from 52, 53 60, & 68] into one of first and second video overlay generators [Fig. 8A; 32 & 42] (see Column 8, Line 18 - Column 10, Line 7). Although the applicants argue that Ranganathan fails to teach routing/switching video data to "only one" display device, such a limitation is nonexistent in pending claim language. Even if Ranganathan arguably discloses routing video to both video overlay generators (as the applicants maintain), this disclosure fully reads upon the claim limitation of routing video data to one video overlay generator.

Secondly, the applicants contend Ranganathan fails to teach video overlay generators. The examiner respectfully disagrees. The applicants are correct in noting that Ranganathan's video overlay generators [Fig. 8A; 32 & 42] are pixel multiplexers; they are incorrect in the assumption that pixel muxes cannot be construed as video overlay generators. Ranganathan expressly discloses, "Pixel muxes 32, 42 independently select either movie overlay data from YUV path 34 or graphics pixels from RGB path 36" (see Column 9, Lines 5-7). In this manner, Ranganathan's pixel muxes "generate" (i.e. produce / beget / cause to occur) overlay data upon their respective output paths (see Figs. 8A & 8B).

Thirdly, the applicants contend Ranganathan fails to teach a "programmable register." The examiner respectfully disagrees. Ranganathan discloses one such programmable register [Fig. 8A; 67] (Column 9, Lines 37-46) providing the full and exact functionality defined by present claim language.

Fourthly, the applicants contend Ranganathan fails to teach display engines responsive to graphics data. The examiner respectfully disagrees. Ranganathan discloses a first display engine [Fig. 8A; 52] responsive to first graphics data [i.e. icon overlay], and a second display engine [Fig. 8A; 53] responsive to second graphics data [i.e. cursor overlay] (Column 9, Lines 5-36).

Fifthly, the applicants contend Ranganathan fails to teach a selectable clock source coupled to a scaler. The examiner respectfully disagrees. Ranganathan discloses, "In other aspects a clock generator generates the pixel clock. The clock generator generates a horizontal line clock by dividing the pixel clock. A vertical clock is generated by dividing the horizontal line clock. The vertical clock indicates when a new frame of pixels is to begin. The new frame includes a plurality of horizontal lines signaled by the horizontal line clock" (see Column 4, Lines 6-14). Additionally, Ranganathan recites, "Movie pixels loaded into movie FIFO 62 are clocked by the video clock to scaler 64 and color-space converter 66" (see Column 8, Lines 57-58).

Sixthly, the applicants contend Ranganathan neglects to teach programming of frame buffer space. The examiner respectfully disagrees. Ranganathan explicitly discloses, "Graphics memory 56 also contains a half-frame buffer 58 which is used to buffer half of the frame being displayed" (see Column 7, Lines 28-29). Ranganathan continues, "A full-frame buffer may be used rather than a half-frame buffer" (see Column 7, Lines 28-29).

Lastly, the applicants contend Ranganathan fails to teach the selection of display-dependent clock signals. The examiner respectfully disagrees. Ranganathan discloses, "FIG. 9 is an alternate embodiment of the dual graphics controller of FIG. 8B which allows for separate refresh rates of the CRT and LCD displays" (see Column 10, Lines 10-12). Moreover, Ranganathan teaches, "the pixel data for the movie window is in YUV format rather than RGB format, as is thus stored separately from the RGB graphics data, either in a separate memory, or in a separate part of the frame buffer graphics memory" (see Column 12, Lines 15-19).

By such reasoning, rejection of the pending claims is deemed necessary, proper, and thereby maintained at this time.


4 November 2003



BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600